High Performance RF Power LDMOSFET Technology for 2.1GHz Power Amplifier Applications

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Abstract:

Silicon RF LDMOSFET technology is demonstrated with excellent RF performance. It achieves high power gain of 14.5db with a high power of 130W at 2.1GHz. Its high efficiency and high linearity makes it highly desired for base station applications. 2mil substrate enables the best-in-class of thermal stability. Low HCI effect, integrated ESD and gold metal ensure high long-term reliability.

Introduction:

In order to build base station equipment that delivers enhanced sensitivity, higher efficiency, lower distortion and increased output power, the RF power amplifier has been challenged intensively. The key component, RF power devices, has been gaining increased attention [1][2][3][5]. Attempts to make better devices have been made continually. Under the stress of cost, in trying to achieve high power levels, designers run the risk of reducing the linearity and efficiency in the amplifier design. It is strongly required to improve the power gain, efficiency, and linearity of the power devices. In the paper, high performance LDMOSFETs with high gain (~14.5db) at 2.1 GHz, high power level (130W, single ended), good linearity over a large dynamic power range, and high drain efficiency (~60%) is demonstrated. With the best-in-class thermal resistance, the powerful device provides very excellent thermal stability. In addition, by proper drain engineering, Hot-Carrier Injection (HCI) issues are suppressed to a negligible level.

Device Structure and Process Technology

The RF LDMOSFET is a Lateral diffused MOS device built on a heavily doped P+ substrate with the top source of the device shorted to the backside and it acts as the RF ground. The poly-silicon gate resistance, being a critical RF parameter, is minimized to give a very low sheet resistance for a poly-silicon gate length of 0.6um. A stepped LDD is optimized by trading-off between drain current capability, reverse feedback capacitance Crss and Hot-Carrier Injection. A dummy gate [4][5] is employed to get a lower Miller capacitance Crss and to make the electric field distribution in the drain side more uniform, ensuring a lower reverse feedback and high breakdown voltage.

Fig.1 shows the top view of device, which is fabricated with modified N-channel MOSFETs technology. Starting with heavily doped P+ substrate, lightly doped thick p-epi was grown to support the drain vertical breakdown voltage. Unique methods of source via have been developed to minimize the source resistance and inductance. Thin gate oxide is formed after the pad oxide is stripped. After the poly gate had been defined, p-body, LDD, and N+ source drain were formed. The dummy gate was defined following a dielectric layer deposition. Thinner source metal and thicker drain metal were made after the windows had been opened. Finally, the wafers were reduced to 2mil before assembling. As shown in Fig. 2, the devices have been input output matched internally.

DC and AC parameters:

To target the Vdd bias of 28V, the blocking voltage of the device was designed to be above 70V. Fig. 3 shows the pulsed DCIV characteristics of 6mm gate width device fabricated as the test structure. It can

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be seen that at Vdd drain bias, the trans-conductance Gm is linear over a wide range of Vgs. For a given gate bias, the drain current is very flat, reflecting a high output resistance of the device. Measurements were also done on the most critical parameter: miller capacitance Crss. Due to the proper design of dummy gate and drain engineering, Crss is significantly reduced. As shown in Fig. 4, Crss is reduced from 2pF to only 1pF at drain bias of 28V. Moreover, the shape of Crss is improved drastically, namely it became much flater over a wider range of Vds for the dummy gate device compared to a no-dummy gate device.

RF Performance:

The maximum available gain vs frequency is shown in Fig. 5. A significant improvement is obtained with the dummy gated devices. Fig. 6 shows the plot of output power, power gain and input power at 2.1 GHz at different quiescent drain current. Clearly, power gain is affected by the Idq. Trade-off between power gain and efficiency is made by the proper choice of Idq, which also affects the gain flatness as a function of input power. As shown in Fig. 7, high gain of 14.5db has been achieved with output power compressed by 1db at 130W, which is obtained with drain efficiency as high as 60%. Linearity was also characterized at 2 tone continuous wave application. Fig. 8 shows the third order Inter-Modulation Distortion (IMD3) vs output power at various Idq. At Idq of 1400mA, IMD3 is lower than –45dbc up to a high output power of 70W. 2-carrier W-CDMA ACPR, IMD3, drain efficiency versus output power is shown in Fig. 9. With 28W output power and maximum IM3 of –35dbc, a drain efficiency of 28.5% is achieved.

Reliability:

Long term reliability of the devices is realized with gold based metalization and ESD protection. Furthermore, the issues of hot-carrier injection (HCI) are resolved by drain engineering. As a result, the HCI induced Idq drift is suppressed. As shown in Fig. 10, in our devices the Id drift is only 3~4% extrapolated to 20 years time for the worst case operating conditions. Even with a higher Vds of 32V, HCI induced Idq drift is less than 5% for 20 years.

Conclusion:

In summary, RF LDMOSFET is demonstrated with excellent RF performance. It achieves high power gain of 14.5db with a high power of 130W at 2.1GHz. Its high efficiency and high linearity makes it highly desired for base station applications. 2mil substrate enables the best-in-class of thermal stability. Low HCI effect, integrated ESD and gold metal ensure high long-term reliability.

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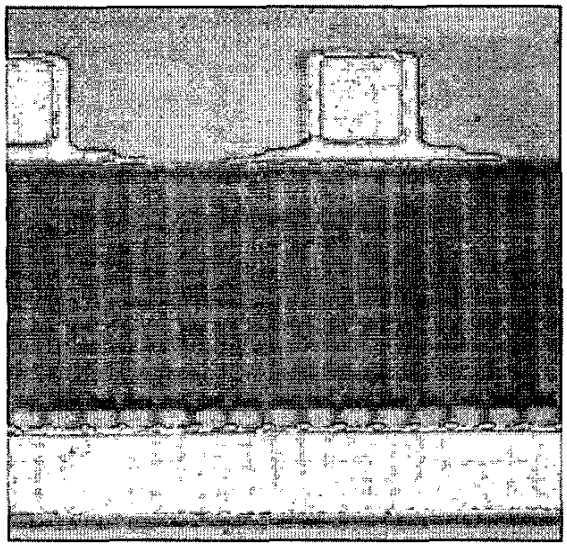

Fig. 1 Top view of finger cells of the device

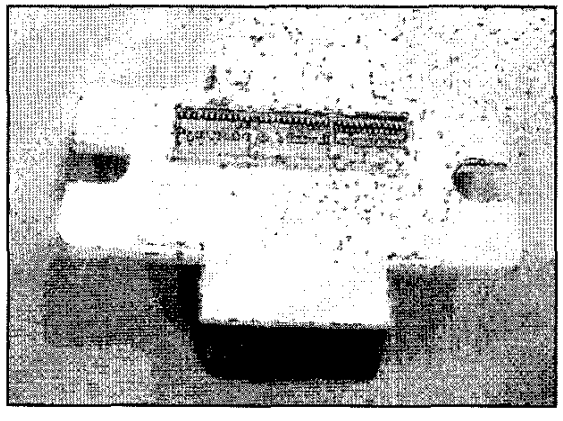

Fig. 2 Photograph of 125W transistor with internal matching

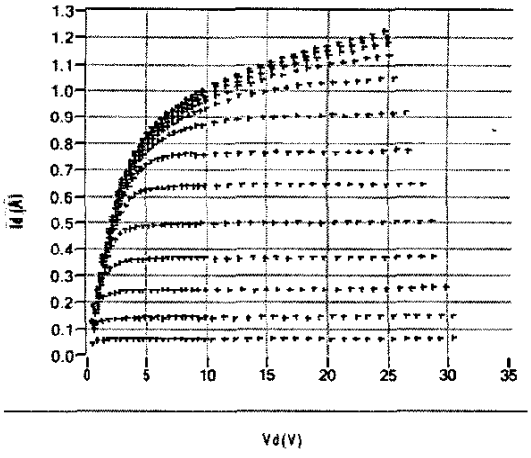

Fig. 3 Pulsed DCIV characteristics collected from test device

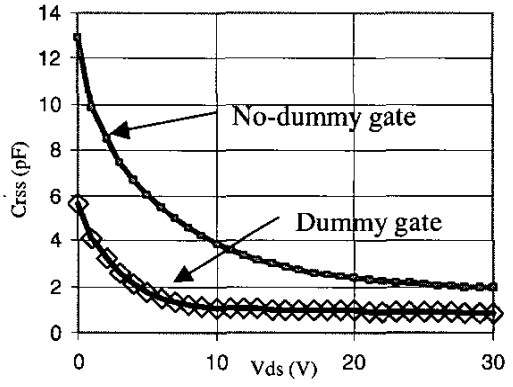

Fig. 4 Crss vs drain bias Vds for device with and without dummy gate

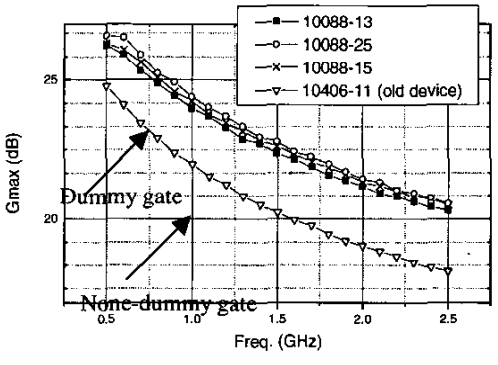

Fig. 5 Measured maximum available gain

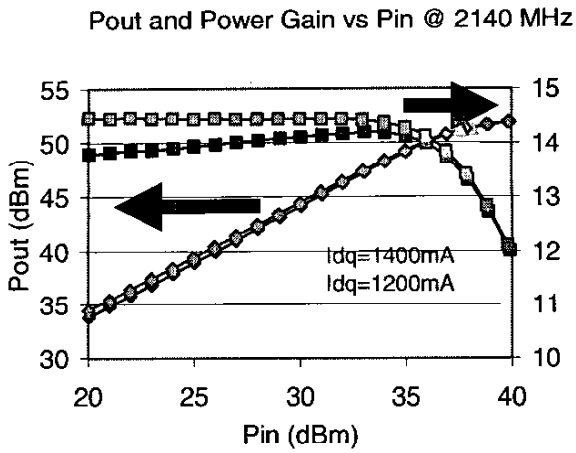

Fig. 6 Characteristics of output power, gain vs input power of 125W device

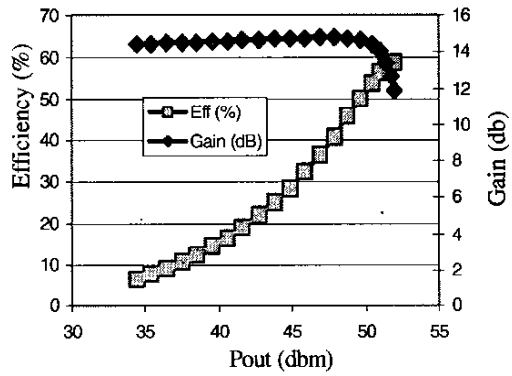

Fig. 7 Measured efficiency, gain vs output power at 2.14 Ghz of 125W transistor

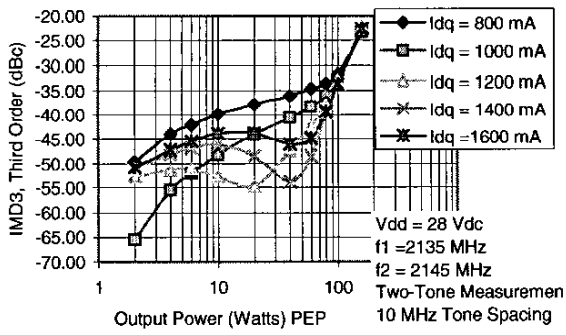

Fig. 8 Two-Tone intermodulation Distortion vs Output power as a function of drain bias

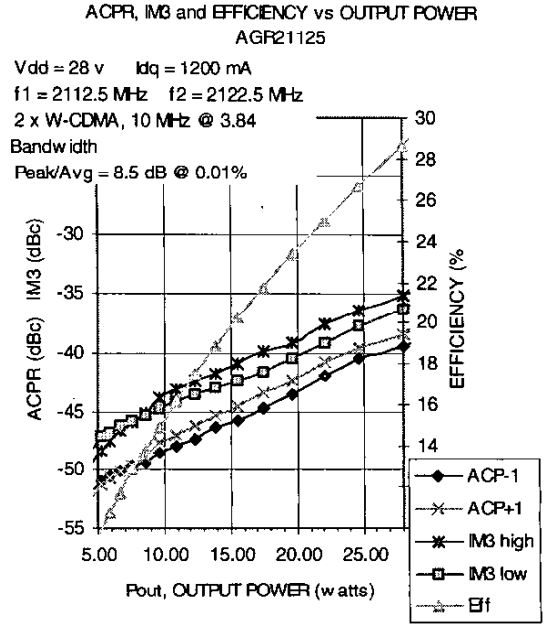

Fig. 9 2-Carrier W-CDMA ACPR, IM3, Drain Efficiency vs output power

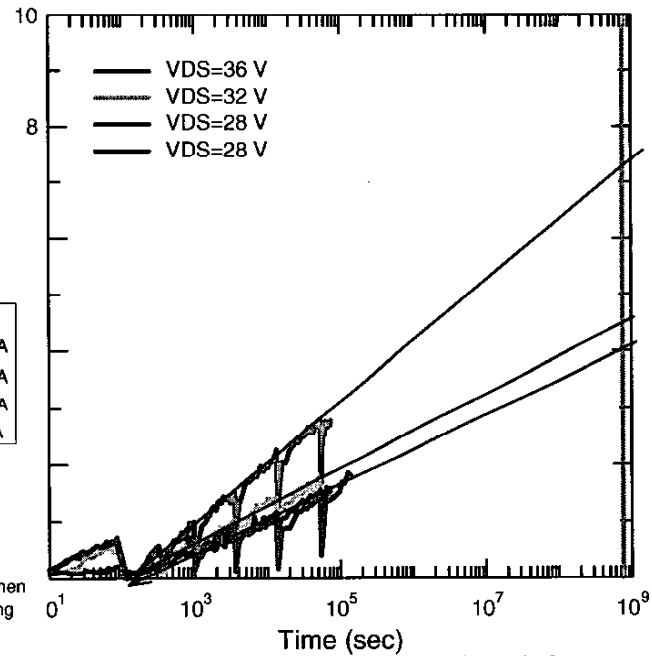

Fig. 10 Quiescent drain current degradation vs stress time at Vds=28, 32, and 36V operation conditions